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(54) **HYBRID THIN FILM TRANSISTOR AND ORGANIC LIGHT EMITTING DISPLAY DEVICE USING THE SAME**

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(57) **ABSTRACT**

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Different types of thin film transistors are disposed on the same flexible substrate and an organic light emitting display using the same includes a display area and a non-display area; a first buffer layer over an entire surface of the flexible substrate; a driving transistor on the buffer layer in the display area, the driving transistor including a polycrystalline silicon (LIPS) layer, a first gate electrode, a first source electrode, and a first drain electrode; a capacitor electrode on the first source electrode of the driving transistor and forming a storage capacitor together with the first source electrode; a switching transistor in the display area to be spaced apart from the driving transistor; and a dummy electrode on the switching transistor, the dummy electrode formed of the same material as the capacitor electrode, and disposed on the same plane as the capacitor.

(21) Appl. No.: **15/652,955**

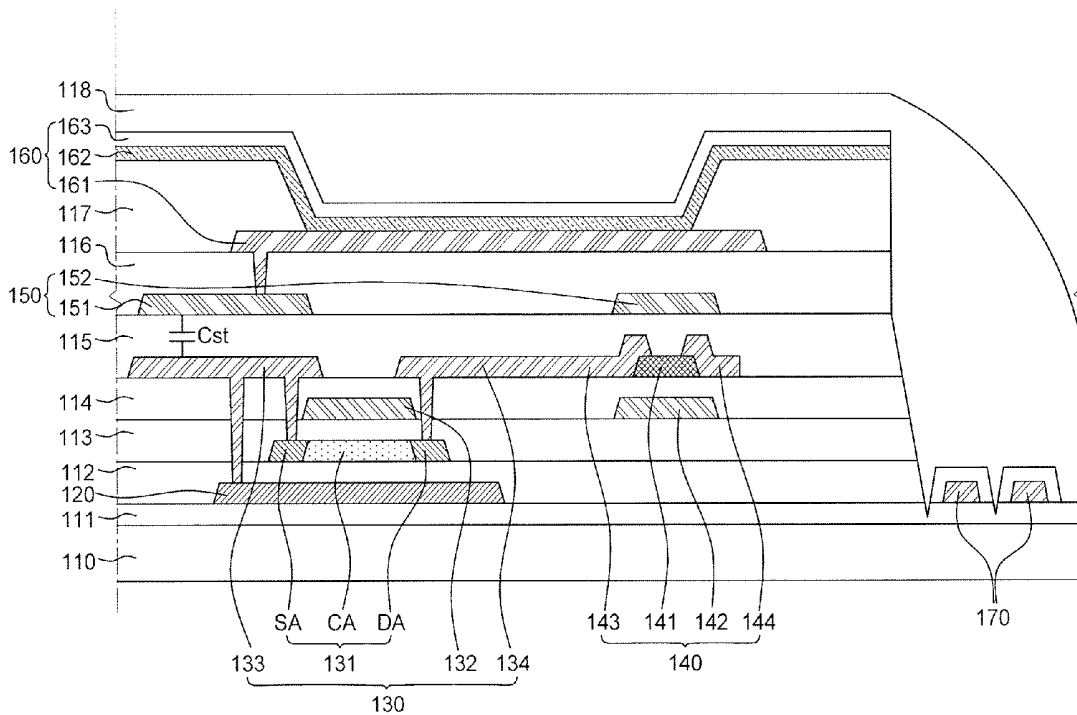
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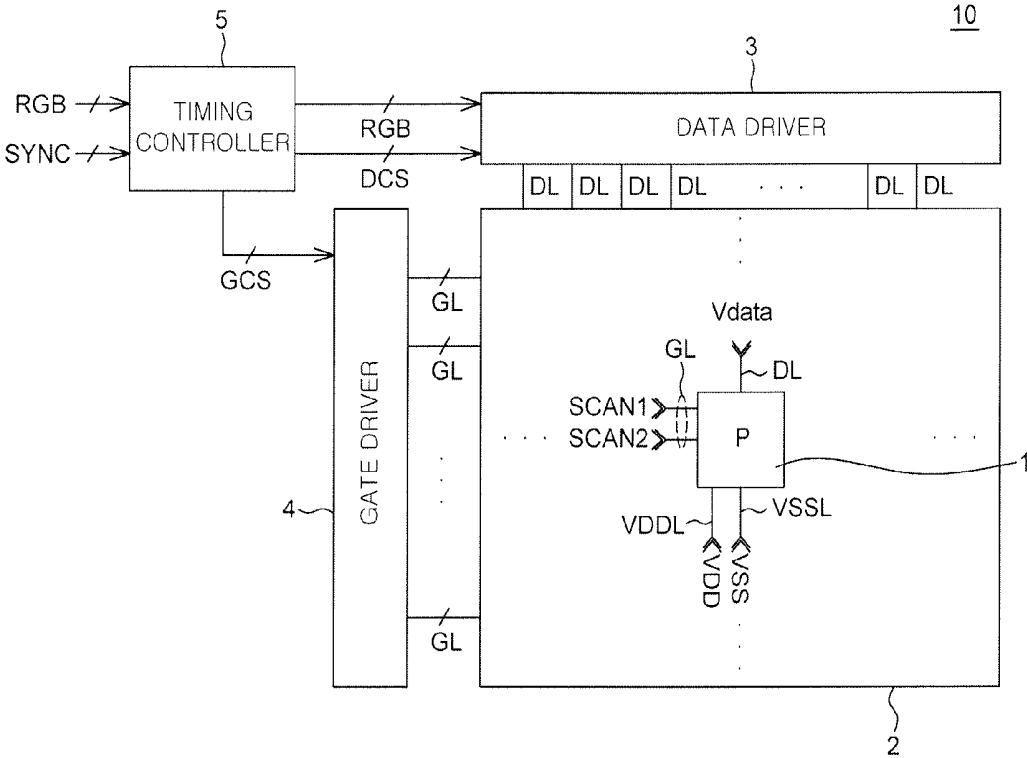


FIG. 1

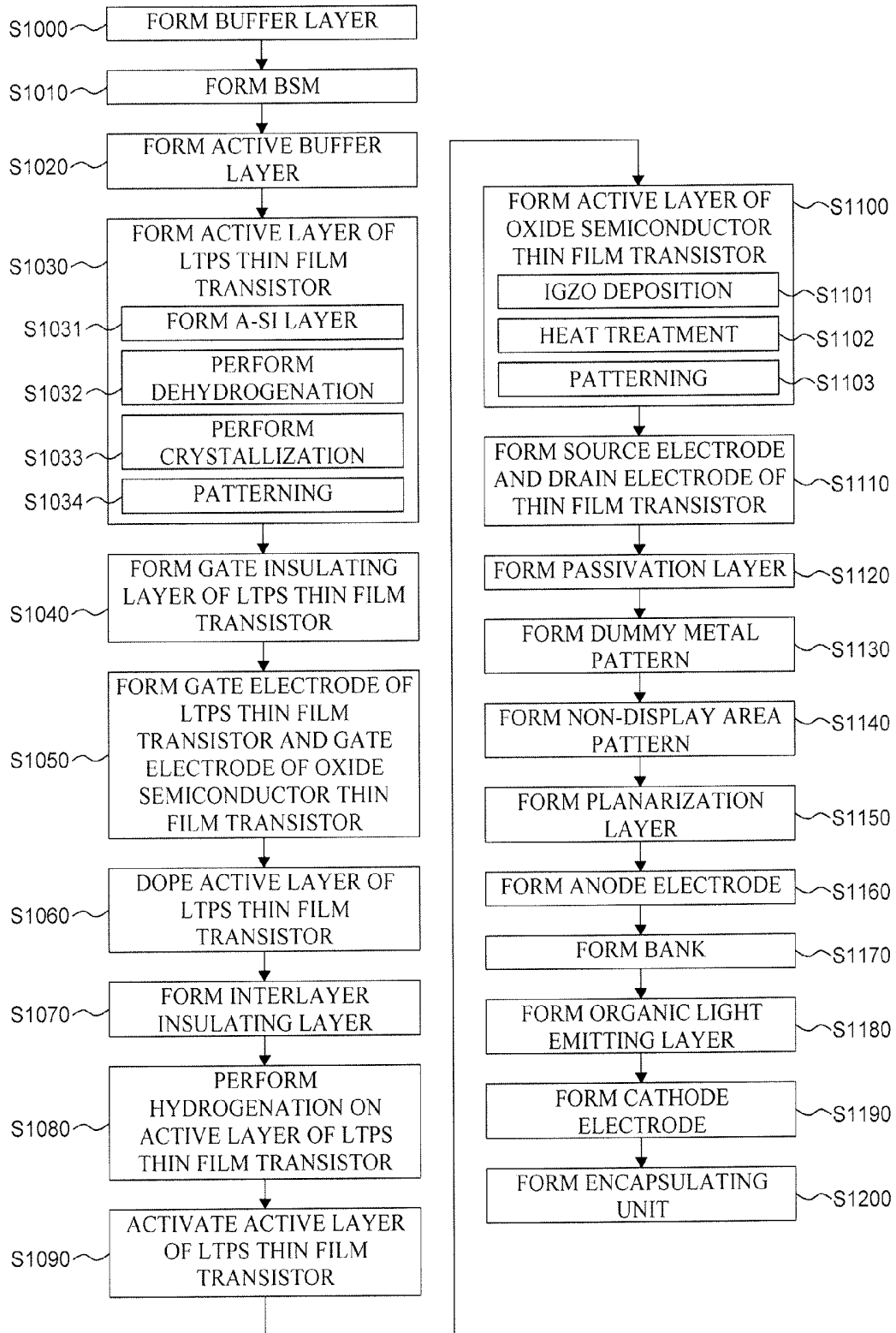


FIG. 3

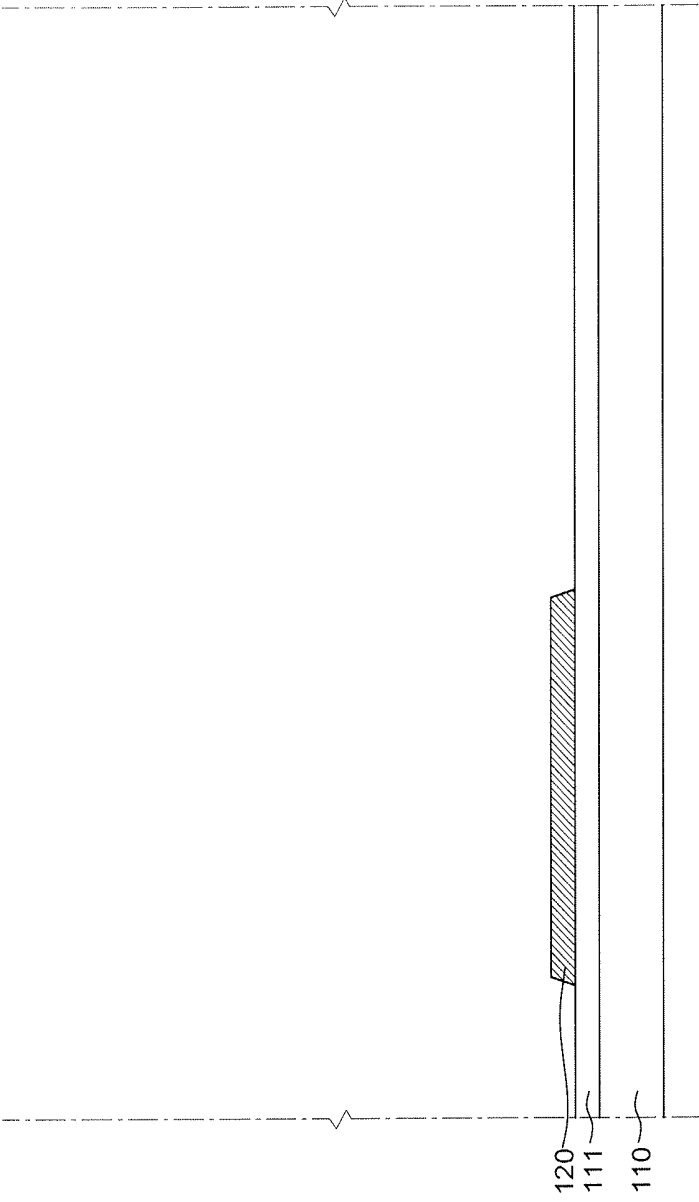


FIG. 4A

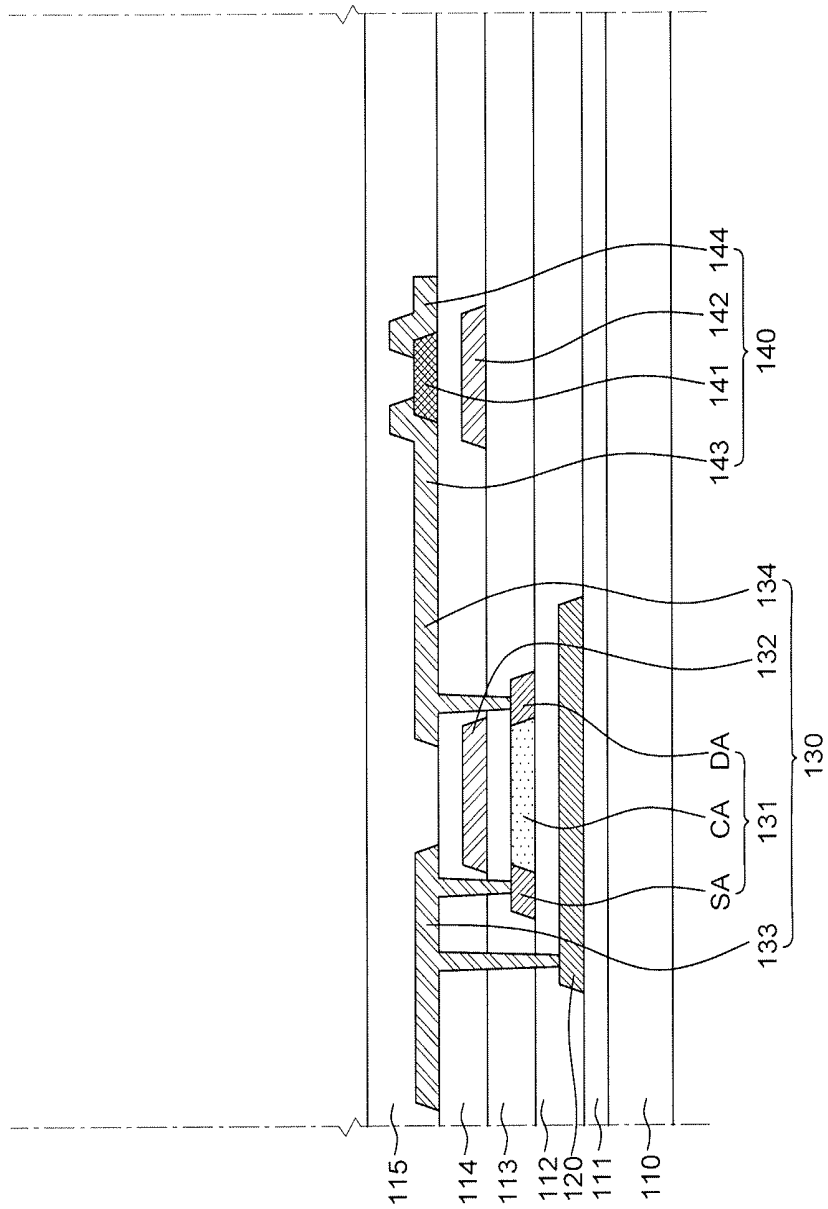


FIG. 4B

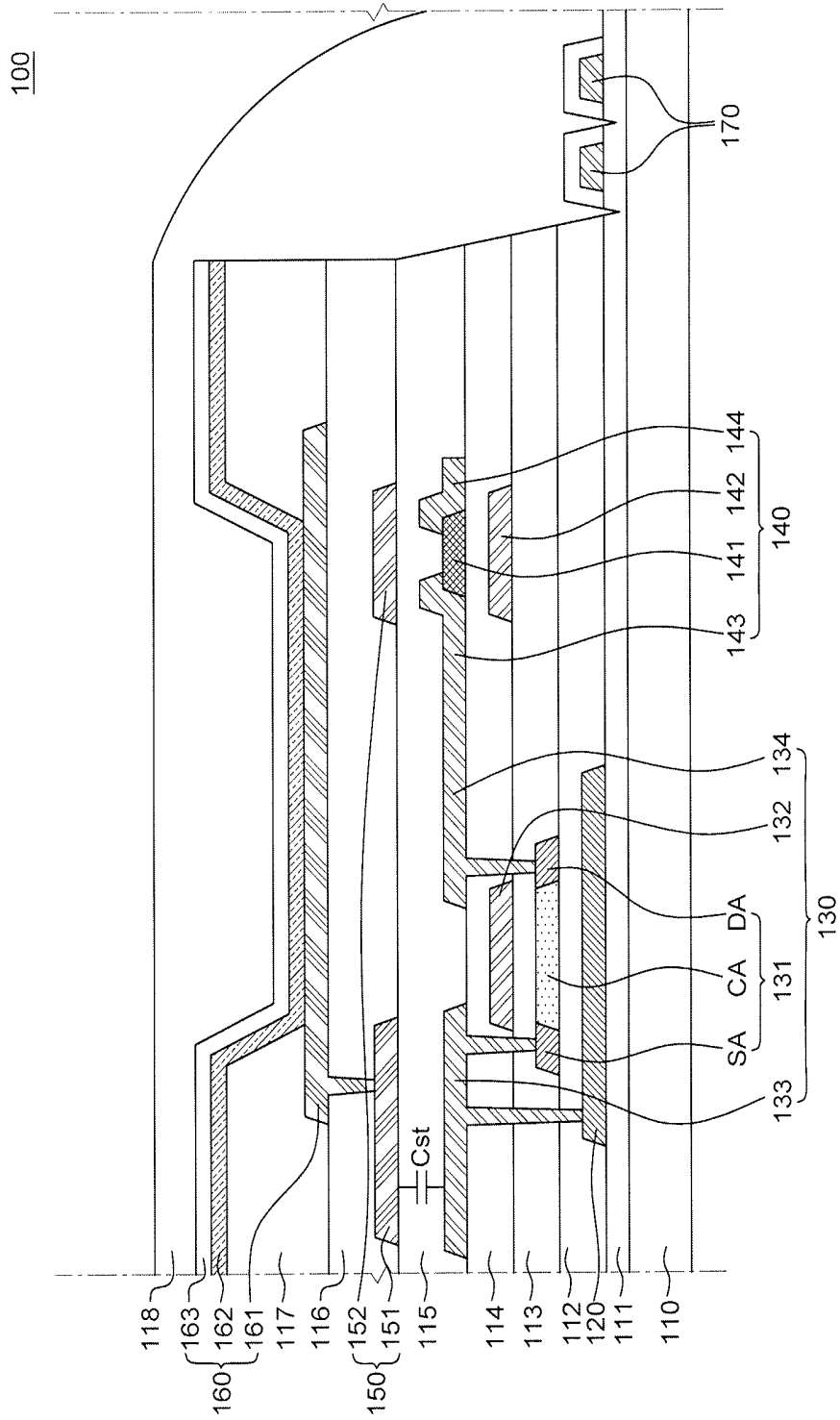


FIG. 4C

**HYBRID THIN FILM TRANSISTOR AND
ORGANIC LIGHT EMITTING DISPLAY
DEVICE USING THE SAME**

CROSS-REFERENCE TO RELATED
APPLICATIONS

[0001] This application claims the priority of Korean Patent Application No. 10-2016-0095249 filed on Jul. 27, 2016, in the Korean Intellectual Property Office, the disclosure of which is incorporated herein by reference into the present application.

BACKGROUND

Field

[0002] The present disclosure relates to a hybrid thin film transistor in which different types of thin film transistors are disposed on the same flexible substrate and an organic light emitting display device using the same.

Description of the Related Art

[0003] The demand for display devices is increasing. As such, thin, light, and high resolution flat panel display devices (FPD) have replaced bulky cathode ray tube (CRT) displays.

[0004] The flat panel display device can be a light crystal display device (LCD), an organic light emitting display device (OLED), or an electrophoretic display device (ED).

[0005] The liquid crystal display device, the organic light emitting display device, and the electrophoretic display device which are actively driven each include a thin film transistor substrate in which thin film transistors allocated in a pixel area disposed in a matrix manner are disposed.

[0006] The liquid crystal display device (LCD) displays an image by adjusting light transmittance of liquid crystal using an electric field applied thereto. The organic light emitting display device displays an image via organic light emitting diodes in pixels arranged in a matrix manner.

[0007] The organic light emitting diode is a self-light emitting element which emits light by itself and is advantageous in terms of a high response speed, high luminous efficiency, high luminance, and a wide viewing angle.

[0008] Specifically, the organic light emitting display device (OLED) which uses a characteristic of an organic light emitting diode with excellent energy efficiency is broadly classified into a passive matrix type organic light emitting display (PMOLED) and an active matrix type organic light emitting display device (AMOLED).

[0009] In the organic light emitting display device, pixels including organic light emitting diodes and pixel circuits are disposed in a matrix form and luminance of an image is adjusted by pixels which are driven in accordance with a gray scale of video data.

[0010] Further, the organic light emitting display device includes a plurality of gate electrode lines, a plurality of data lines, a plurality of power lines, and a plurality of pixels which is connected to the above-mentioned lines to be disposed in a matrix form. Each pixel includes an organic light emitting diode configured by an organic light emitting layer between an anode and a cathode and a pixel circuit which independently drives the organic light emitting diode. The pixel circuit is mainly configured by a switching transistor which transmits a data signal, a driving transistor

which drives the organic light emitting diode in accordance with the data signal, and one capacitor which maintains a data voltage. The switching transistor charges the data voltage into the capacitor in response to a scan pulse. The driving transistor adjusts a light emission amount of the organic light emitting diode by controlling a current amount supplied to the organic light emitting diode in accordance with the data voltage charged in the capacitor. Further, a turn-on time of the switching transistor may be shorter than that of the driving transistor. The turn-on time of the transistor is related to power consumption of the organic light emitting display device.

[0011] In accordance with the active development of personal electronic devices, display devices have been also developed as products which are superior in portability and wearability. As described above, in order to apply the display device to the portable or wearable device, a display device with low power consumption is required. However, technologies related to the display devices developed so far have limitations in realizing low power consumption.

[0012] Therefore, in recent years, in order to overcome the above-described problems, there is a necessity for a new pixel structure and a new organic light emitting display device which can drive the pixels with low power consumption.

SUMMARY

[0013] The inventors of the present disclosure invented a new pixel structure and a new organic light emitting display device which drive pixels of the organic light emitting display device with low power consumption as described above.

[0014] Therefore, an aspect of the present disclosure is to provide a new pixel structure and a new organic light emitting display device in which a driving transistor with a low temperature polycrystalline silicon (LTPS) layer as an active layer and a switching transistor with an oxide semiconductor layer as an active layer are formed.

[0015] Another aspect of the present disclosure is to provide a new pixel structure and a new organic light emitting display device in which a dummy metal pattern is formed on a switching transistor including an oxide semiconductor layer so that a switching transistor includes a dual gate electrode structure, thereby improving bias temperature stress and shielding external light which is incident onto an upper portion and a lower portion of a channel.

[0016] According to an aspect of the present disclosure, there is provided an organic light emitting display device that includes a flexible substrate including a display area and a non-display area, a first buffer layer is disposed over an entire surface of the flexible substrate, a driving transistor on the buffer layer in the display area, the driving transistor including a polycrystalline silicon (LIPS) layer, a first gate electrode, a first source electrode, and a first drain electrode, and a capacitor electrode on the first source electrode of the driving transistor, the capacitor electrode forming a storage capacitor together with the first source electrode.

[0017] The organic light emitting display device may further include a switching transistor in the display area to be spaced apart from the driving transistor, the switching transistor including an oxide semiconductor layer, a second gate electrode, a second source electrode, and a second drain electrode and a dummy electrode on the switching transistor, the dummy electrode formed of the same material as the

capacitor electrode, and disposed on the same plane as the capacitor. The dummy electrode may be a third gate electrode of the switching transistor.

[0018] According to another aspect of the present disclosure, an organic light emitting display device includes a flexible substrate including a display area and a non-display area, a driving transistor in the display area, the driving transistor having a polycrystalline silicon (LIPS) layer as an active layer, and a switching transistor in the display area, the switching transistor disposed to be spaced apart from the driving transistor.

[0019] The switching transistor includes a first gate electrode, an oxide semiconductor layer overlapping the gate electrode, a source electrode in contact with one side of the oxide semiconductor layer, a drain electrode in contact with the other side of the oxide semiconductor layer; and a second gate electrode connected to the first gate electrode.

[0020] According to the organic light emitting display device of the present disclosure, the driving transistor with the polycrystalline silicon (LIPS) layer as an active layer and the switching transistor with an oxide semiconductor layer as an active layer are formed on the same substrate, so that a drawback of any one of the thin film transistors is compensated by the other thin film transistor. Specifically, the oxide semiconductor thin film transistor is provided so that it is possible to provide an organic light emitting display device suitable for a portable and/or wearable apparatus by realizing low-speed driving and reducing the power consumption. Further, a source electrode of the driving transistor and some electrodes of a dummy metal pattern form a storage capacitor C_{st} to increase the storage capacitor C_{st} of the display device with high resolution. Further, the dummy metal pattern is formed on the switching transistor to improve a bias temperature stress and shield external light which is incident onto an upper portion and a lower portion of a channel, using a switching transistor with a dual gate electrode structure.

BRIEF DESCRIPTION OF DRAWINGS

[0021] The above and other aspects, features and other advantages of the present disclosure will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings, in which:

[0022] FIG. 1 is a diagram illustrating an organic light emitting display device according to an embodiment of the present disclosure;

[0023] FIG. 2 is a cross-sectional view schematically illustrating a pixel structure illustrated in FIG. 1 according to an embodiment of the present disclosure;

[0024] FIG. 3 is a flowchart illustrating a manufacturing process of a pixel illustrated in FIG. 1 according to an embodiment of the present disclosure; and

[0025] FIGS. 4A to 4C are cross-sectional views of a process for explaining a manufacturing process of a pixel illustrated in FIG. 1 according to an embodiment of the present disclosure.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0026] Advantages and characteristics of the present disclosure and a method of achieving the advantages and characteristics will be clear by referring to exemplary embodiments described below in detail together with the

accompanying drawings. However, the present disclosure is not limited to exemplary embodiment disclosed herein but will be implemented in various forms. The exemplary embodiments are provided by way of example only so that a person of ordinary skilled in the art can fully understand the disclosures of the present disclosure and the scope of the present disclosure. Therefore, the present disclosure will be defined only by the scope of the appended claims.

[0027] The shapes, sizes, ratios, angles, numbers, and the like illustrated in the accompanying drawings for describing the exemplary embodiments of the present disclosure are merely examples, and the present disclosure is not limited thereto.

[0028] Further, in the following description of the present disclosure, a detailed explanation of known related technologies may be omitted to avoid unnecessarily obscuring the subject matter of the present disclosure. The terms such as “including,” “having,” and “consist of” used herein are generally intended to allow other components to be added unless the terms are used with the term “only”. Any references to singular may include plural unless expressly stated otherwise.

[0029] Components are interpreted to include an ordinary error range even if not expressly stated. When the position relation between two parts is described using the terms such as “on”, “above”, “below”, and “next”, one or more parts may be positioned between the two parts unless the terms are used with the term “immediately” or “directly” is not used.

[0030] When an element or layer is disposed “on” other element or layer, another layer or another element may be interposed directly on the other element or therebetween.

[0031] Although the terms “first”, “second”, and the like are used for describing various components, these components are not confined by these terms. These terms are merely used for distinguishing one component from the other components. Therefore, a first component to be mentioned below may be a second component in a technical concept of the present disclosure.

[0032] Like reference numerals generally denote like elements throughout the specification.

[0033] A size and a thickness of each component illustrated in the drawing are illustrated for convenience of description, and the present disclosure is not limited to the size and the thickness of the component illustrated.

[0034] The features of various embodiments of the present disclosure can be partially or entirely bonded to or combined with each other and can be interlocked and operated in technically various ways as understood by those skilled in the art, and the embodiments can be carried out independently of or in association with each other.

[0035] In the present disclosure, a transistor may be a P type transistor or an N type transistor. In the following exemplary embodiment, the transistor will be configured as an N type transistor for the convenience of description.

[0036] Hereinafter, an organic light emitting display device according to an exemplary embodiment of the present disclosure and a driving method thereof will be described in detail with reference to the accompanying drawings.

[0037] FIG. 1 is a diagram illustrating an organic light emitting display device according to an exemplary embodiment of the present disclosure. All the components of the

organic light emitting display device according to all embodiments of the present disclosure are operatively coupled and configured.

[0038] An organic light emitting display device 10 illustrated in FIG. 1 includes a display panel 2 in which a plurality of gate lines GL and a plurality of data lines DL are disposed, whereby a pixel 1 is repeatedly arranged in a matrix layout, a gate driver 4 which transmits a driving signal of the pixel 1 to the plurality of gate lines GL, a data driver 3 which transmits a driving voltage of the pixel 1 to the plurality of data lines DL, and a timing controller 5 which aligns image data RGB input from the outside to supply the image data to the data driver 3 and outputs a gate control signal GCS and a data control signal DCS to control the gate driver 4 and the data driver 3.

[0039] According to the exemplary embodiment of the present disclosure, each pixel 1 among the plurality of pixels includes an organic light emitting diode (OLED) and a pixel driving circuit which includes a driving transistor supplying a driving current to the organic light emitting diode (OLED) to independently drive the organic light emitting diode (OLED). The pixel driving circuit may compensate an electrical characteristic deviation of the driving transistor such as a threshold voltage V_{th} and a mobility and reduce a luminance deviation between pixels 1 caused by a difference between currents supplied to the organic light emitting diode (OLED). The pixel 1 according to the exemplary embodiment of the present disclosure will be described in detail below with reference to FIGS. 2 to 4C.

[0040] The display panel 2 includes a plurality of gate lines GL and a plurality of data lines DL which intersect each other and a plurality of pixels 1 is disposed near the lines GL and DL. Each pixel 1 includes an organic light emitting diode OLED and a pixel driving circuit. The pixel 1 is connected to the gate line GL, the data line DL, a first voltage (VDD) supply line VDDL and a second voltage (VSS) supply line VSSL.

[0041] The gate driver 4 supplies a plurality of gate electrode signals to the plurality of gate lines GL in accordance with a plurality of gate control signals GCS supplied from the timing controller 5. The plurality of gate electrode signals includes first and second scan signals SCAN1 and SCAN 2 and these signals are supplied to the pixels 1 through the plurality of gate lines GL. The first voltage VDD is a high potential voltage and is relatively higher than a second voltage VSS which is a low potential voltage. The second voltage VSS may be a ground voltage.

[0042] The data driver 3 converts digital image data RGB input from the timing controller 5 into a data voltage V_{data} using a reference gamma voltage in accordance with the plurality of data control signals DCS supplied from the timing controller 5. Further, the data driver 3 supplies the converted data voltage V_{data} to the plurality of data lines DL. In the meantime, the data driver 3 outputs the data voltage V_{data} during a programming period of each pixel 1.

[0043] The timing controller 5 aligns the image data RGB input from the outside in accordance with a size and a resolution of the display panel 2 to supply the image data to the data driver 3. The timing controller 5 generates a plurality of gate control signals GCS and a plurality of data control signals DCS using synchronization signals SYNC input from the outside, for example, a dot clock DCLK, a data enable signal DE, a horizontal synchronization signal Hsync, and a vertical synchronization signal Vsync. The

plurality of generated gate control signals GCS and the plurality of generated data control signals DCS are supplied to the gate driver 4 and the data driver 3, respectively, to control the gate driver 4 and the data driver 3.

[0044] Hereinafter, a pixel according to an exemplary embodiment of the present disclosure will be described in detail. FIG. 2 is a cross-sectional view schematically illustrating a pixel 1 structure illustrated in FIG. 1.

[0045] Each pixel 1 structure of an organic light emitting display device will be described with reference to FIG. 2. As illustrated in FIG. 2, the pixel 1 according to the exemplary embodiment of the present disclosure includes a lower substrate 110, a buffer layer 111, a bottom shield metal (BSM) 120, an active buffer layer 112, an LTPS thin film transistor 130, an oxide semiconductor thin film transistor 140, a dummy metal layer 150, an organic light emitting diode 160, and a signal line 170.

[0046] Further, the pixel 1 according to the exemplary embodiment of the present disclosure includes a gate insulating layer 113, an interlayer insulating layer 114, a passivation layer 115, a planarization layer 116, a bank 117, and an encapsulation unit 118.

[0047] The lower substrate 110 may be formed of plastic polymer material such as polyimide (PI). On the lower substrate 110, a plurality of switching transistors ST and a driving transistor DT related to the driving of the organic light emitting diode OLED.

[0048] The lower substrate 110 may be attached onto an auxiliary substrate. The auxiliary substrate may be configured by a glass substrate and a sacrificial layer. The auxiliary substrate may be separated from the lower substrate 110 on which an organic light emitting diode is formed, by a laser release process.

[0049] Further, the lower substrate 110 may include a display area and a non-display area. In the display area, a plurality of pixel areas is disposed in a matrix manner. In the pixel area, display elements for a displaying function are disposed. The non-display area may be disposed in the vicinity of the display area and driving elements for driving display elements formed in the pixel area may be disposed therein. Further, a part of the non-display area of the lower substrate 110 may be bent if necessary.

[0050] The display area may be divided into a first area and a second area which is spaced apart from the first area. The pixel 1 of the organic light emitting display device according to the exemplary embodiment of the present disclosure includes a first thin film transistor disposed in the first area and a second thin film transistor disposed in the second area, on the lower substrate 110. The first thin film transistor may be the LTPS thin film transistor 130 and the second thin film transistor may be the oxide semiconductor thin film transistor 140. Specifically, when a plurality of thin film transistors is included in a unit pixel area, the first thin film transistor and the second thin film transistor may be disposed to be adjacent to each other. Specifically, the first thin film transistor including a polycrystalline semiconductor material may be applied to the driving thin film transistor and the second thin film transistor including the oxide semiconductor material may be applied to the switching thin film transistor.

[0051] Further, the first thin film transistor is a thin film transistor for a gate driving element formed in the non-display area and the second thin film transistor may be a thin film transistor for a display element disposed in the pixel

area of the display area. Further, when the gate driving element is formed in the non-display area, the gate driving element may be implemented by a C-MOS type thin film transistor including the polycrystalline silicon LIPS layer. That is, both a P-MOS type thin film transistor and a N-MOS type thin film transistor including the polycrystalline silicon LIPS layer are formed in a gate driver in the non-display area. In this case, for the N-MOS type, a plurality of mask process for forming a low density doping area is required. Here, the gate driving element may be configured by a hetero thin film transistor in which the N-MOS type thin film transistor including the polycrystalline silicon LIPS layer is replaced with a thin film transistor including an oxide semiconductor layer. By doing this, the low density doping area may be avoided, so that it is advantageous in that the number of mask processes may be reduced.

[0052] As described above, the substrate including the hetero thin film transistor may be applied to the organic light emitting display device. For example, in the case of the organic light emitting display device, the second thin film transistor may be a switching thin film transistor which selects a pixel and the first thin film transistor may be a driving thin film transistor which drives the selected pixel. In some cases, the second thin transistor and the first thin film transistor may be configured in an opposite manner.

[0053] Next, the buffer layer 111 is formed on the entire surface of the lower substrate 110.

[0054] That is, the buffer layer 111 can be entirely formed over the display area and the non-display area of the lower substrate 110. The buffer layer 111 may have a structure in which a plurality of thin films is deposited. Here, it is described that the buffer layer 111 is a single layer for the convenience of description. Silicon oxide (SiO_x) which does not specifically affect the elements may be used for the buffer layer 111.

[0055] Further, as illustrated in FIG. 2, a groove may be formed in a part of the buffer layer 111 located in the non-display area to minimize cracks or other irregularities which may be caused during the bending.

[0056] Next, the BSM 120 is selectively formed only in a necessary area on the buffer layer 111. Further, the BSM 120 may be formed using molybdenum (Mo) material. The BSM 120 is located on the buffer layer 111 to overlap the LTPS thin film transistor 130 which is a driving thin film transistor of the pixel 1.

[0057] The BSM 120 may fundamentally block a potential from generating on the surface of the lower substrate 110 and light which is incident from the outside.

[0058] More specifically, in the pixel 1 according to the exemplary embodiment of the present disclosure, the active layers of various transistors including the driving transistor DT may be damaged due to the laser release process. Further, a negative charge trap is generated on the sacrificial layer due to laser and light incident from the outside and thus positive (+) charges may move from polyimide PI which forms the lower substrate 110 toward the sacrificial layer. By doing this, the potential on the surface of the lower substrate 110 may be increased. As a result, current which flows through the transistor may be reduced.

[0059] Further, when the LTPS thin film transistor 130 is turned off, a source electrode 133 of the LTPS thin film transistor 130 which is connected to the organic light emitting diode OLED is maintained to be floated. In this case, as the potential of the surface of the lower substrate 110 is

increased, a parasitic capacitance may be generated between the lower substrate 110 and the source electrode 133 of the LIPS thin film transistor 130. The source electrode 133 may be consistently affected by the parasitic capacitance. Therefore, the current which flows through the source electrode of the LIPS thin film transistor 130 may be changed by the parasitic capacitance, so that a residual-image may be generated even at the time of restoration.

[0060] Further, after performing the laser release process, when the pixel 1 of the organic light emitting display device 100 including the lower substrate 110 which is formed of a plastic polymer material such as polyimide (PI) is driven, heat may be generated in the lower substrate 110. As a result, charged particles generated in the lower substrate 110 may upwardly move. The charged particles affect the active layers of the thin film transistors, which may lower reliability of the organic light emitting display device 100.

[0061] Therefore, as illustrated in FIG. 2, the BSM 120 is electrically connected to the source electrode 133 of the LTPS thin film transistor 130 to minimize influence of the charges flowing through a channel of the thin film transistor which drives the pixel 1. As a result, a current drop phenomenon in which the driving current of the thin film transistor is lowered, restoration residual image problem and reliability of the OLED display device 100 may be solved.

[0062] Next, an active buffer layer 112 which encloses the BSM 120 and protects the active layer of the LTPS thin film transistor 130 is located on the buffer layer 111. The active buffer layer 112 is formed only in the display area of the lower substrate 110. The active buffer layer 112 may be formed of the same material as the buffer layer 111.

[0063] Next, the LTPS thin film transistor 130 is located on the active buffer layer 112. The LTPS thin film transistor 130 may be configured by an active layer 131, a gate electrode 132, the source electrode 133, and a drain electrode 134.

[0064] The active layer 131 of the LTPS thin film transistor 130 is formed of a polycrystalline silicon LTPS material. The LTPS material has a high mobility (100 cm²/Vs or higher), so that energy power consumption is lower and reliability is excellent. Therefore, the LTPS material may be applied to a gate driver for a driving element driving thin film transistors for a display element and/or a multiplexer (MUX). Alternatively, the LTPS material may be applied to the driving thin film transistor in the pixel in the organic light emitting display device 100. When the semiconductor layer is formed of the LTPS material, an impurity injecting process and a high temperature heat treatment process are required. In contrast, when the semiconductor layer is formed of an oxide semiconductor material, the process is performed at a relatively low temperature. Accordingly, it is desirable that after forming the LTPS layer in which the process is performed under a severe condition, the oxide semiconductor layer is formed later. Further, for the simplification of the manufacturing process, it is desirable that components of the LIPS thin film transistor 130 including the LIPS layer and the oxide semiconductor thin film transistor 140 including the oxide semiconductor layer are formed on the same layer. For example, it is desirable that the gate electrode 132 of the LIPS thin film transistor 130 and the gate electrode 142 of the oxide semiconductor thin film transistor 140 are formed of the same metal material on the same layer and the source-drain electrode of each thin film transistor is formed of the same metal material on the

same layer. Specifically, in order to secure the characteristic of the semiconductor element, it is desirable to form the LIPS thin film transistor to have a top-gate structure which precisely defines a channel area.

[0065] The active layer **131** is formed on a top surface of the active buffer layer **112**. The active layer **131** includes a channel area CA of the LIPS thin film transistor **130**. The channel area CA is defined as an area where the gate electrode **132** and the active layer **131** overlap each other. Since the gate electrode **132** overlaps a central part of the LIPS thin film transistor **130**, the central part of the LIPS thin film transistor **130** serves as a channel area CA. Both sides of the channel area CA are doped with impurities and are defined as a source area SA and a drain area DA.

[0066] A doping area including the source area SA and the drain area DA is defined by injecting impurities. Each of the source area SA and the drain area DA may include a high density doping area HDD and a low density doping area LDD.

[0067] Further, the active layer **131** is formed by performing low-temperature crystallization on a polycrystalline semiconductor material such as polysilicon. When the LIPS thin film transistor **130** is the driving thin film transistor DT, the LIPS thin film transistor may have a characteristic suitable for performing a high speed driving process. For example, a P-MOS or N-MOS type thin film transistor may be used or a C-MOS type thin film transistor including both the P-MOS and N-MOS thin film transistors may be provided. The P-MOS, the N-MOS and/or the C-MOS type thin film transistors may include a polycrystalline semiconductor material such as polycrystalline silicon (poly-silicon).

[0068] Further, the gate electrode **132** is formed to overlap the channel area CA of the active layer **131**. As a result, the LIPS thin film transistor **130** may have a top-gate structure.

[0069] Further, as illustrated in FIG. 2, the source electrode **133** of the LIPS thin film transistor **130** is in contact with the doping area of the active layer **131** and is electrically connected to the organic light emitting diode **160**. Further, the source electrode **133** may be electrically connected to the BSM **120**. The drain electrode **134** of the LIPS thin film transistor **130** is electrically connected to the source electrode of the oxide semiconductor thin film transistor **140**.

[0070] Next, the gate insulating layer **113** of the LIPS thin film transistor **130** is formed on the active layer **131** of the LIPS thin film transistor **130** in the display area of the lower substrate **110**. The gate insulating layer **113** may be formed of silicon nitride SiNx or silicon oxide SiOx. In consideration of stability and characteristic of the elements, the gate insulating layer **113** may have a thickness of approximately 1000 Å to 1500 Å. When the gate insulating layer **113** is formed of silicon nitride SiNx, a large amount of hydrogen may be contained in the gate insulating layer **113** due to the manufacturing process. The hydrogen may be diffused to the outside of the gate insulating layer **113** in the subsequent process so that the gate insulating layer **113** may be formed of a silicon oxide (SiOx) material.

[0071] Next, the oxide semiconductor thin film transistor **140** is located on the gate insulating layer **113** in the display area of the lower substrate **110**. The oxide semiconductor thin film transistor **140** may be configured by an active layer **141**, a gate electrode **142**, a source electrode **143**, and a drain electrode **144**.

[0072] Further, as illustrated in FIG. 2, the gate electrode **142** of the oxide semiconductor thin film transistor **140** is formed on the gate insulating layer **113**.

[0073] The active layer **141** of the oxide semiconductor thin film transistor **140** is formed of an oxide semiconductor material. For example, the oxide semiconductor material such as indium gallium zinc oxide (IGZO), indium gallium oxide (IGO), and indium zinc oxide (IZO) may be included. The oxide semiconductor material has a low off-current characteristic so that a voltage maintain period of the pixel is long. Therefore, the oxide semiconductor material is suitable for a display device which requires low speed driving and low power consumption. When the oxide semiconductor material is contained, in consideration of a structure in which different types of thin film transistors according to the exemplary embodiment of the present disclosure are included on one substrate, the active layer may have a bottom gate structure which may more efficiently secure the stability of the element.

[0074] The active layer **141** of the oxide semiconductor thin film transistor **140** is located on the gate electrode **142**. The source electrode **143** and the drain electrode **144** of the oxide semiconductor thin film transistor **140** are in electrical contact with the active layer **141**. Further, the source electrode **143** is connected to the drain electrode **134** of the LTPS thin film transistor **130**.

[0075] Further, the signal line **170** may be formed of the same material as the source electrode **143** and the drain electrode **144** of the oxide semiconductor thin film transistor in the non-display area of the lower substrate **110**.

[0076] Further, the gate electrode **142** of the oxide semiconductor thin film transistor **140** is simultaneously formed of the same material as the gate electrode **132** of the LTPS thin film transistor **130** on the same plane. Further, the gate electrode **142** of the oxide semiconductor thin film transistor **140** may be formed of the same material as the BSM **120**.

[0077] Next, the interlayer insulating layer **114** is located on the gate electrode **132** of the LTPS thin film transistor **130** and the gate electrode **142** of the oxide semiconductor thin film transistor **140**, in the display area of the lower substrate **110**. The interlayer insulating layer **114** may have a dual layered structure in which a nitride film SIN including silicon nitride SiNx and an oxide film SIO including silicon oxide SiOx are sequentially deposited. The interlayer insulating layer **114** is formed prior to a subsequent heat treatment process of an activating process and a hydrogenating process on the active layer **131** of the LTPS thin film transistor **130**.

[0078] The nitride film SIN of the interlayer insulating layer **114** diffuses hydrogen contained therein through the subsequent heat treatment process to be deposited to perform the hydrogenating process on the active layer **131** of the LTPS thin film transistor **130** containing the polycrystalline silicon. The hydrogenating process refers to a process in which incompletely coupled spaces are filled with hydrogen through the activating process on the active layer **131** of the LTPS thin film transistor **130**.

[0079] In contrast, the oxidation film SIO of the interlayer insulating layer **114** is deposited in order to suppress hydrogen discharged from the nitride film SIN by the subsequent heat treatment process from being excessively diffused to the semiconductor material of the oxide semiconductor thin film transistor **140**, that is, the active layer **141**.

[0080] For example, the hydrogen discharged from the nitride film SIN of the interlayer insulating layer 114 may be diffused to the active layer 131 of the LIPS thin film transistor 130 disposed with the gate insulating layer 113 therebetween. Therefore, the nitride film SIN may be deposited directly on the gate insulating layer 113. Accordingly, the oxide film SIO may be preferably deposited on the nitride film SIN. In consideration of the manufacturing process, the entire thickness of the interlayer insulating layer 114 may be 2000 Å to 6000 Å. Therefore, each thickness of the nitride film SIN and the oxide film SIO may be 1000 Å to 3000 Å. Further, a large amount of hydrogen in the nitride film SIN of the interlayer insulating layer 114 may be diffused to the active layer 141 of the oxide semiconductor thin film transistor 140. Specifically, the oxide film SIO of the interlayer insulating layer 114 is provided to adjust the diffusing degree of hydrogen which is discharged from the nitride film SIN so that the thickness of the oxide film SIO may be larger than that of the gate insulating layer 113.

[0081] Further, the oxide film SIO of the interlayer insulating layer 114 suppresses moving of hydrogen from the nitride film SIN containing a relatively large amount of hydrogen to the active layer 141 of the oxide semiconductor thin film transistor 140. When the hydrogen moves from the nitride film SIN to the active layer 141 of the oxide semiconductor thin film transistor 140, the active layer 141 of the oxide semiconductor thin film transistor 140 is reduced and a threshold voltage V_{th} of the oxide semiconductor thin film transistor 140 is changed.

[0082] Therefore, the interlayer insulating layer 114 having a dual layered structure in which the nitride film SIN including silicon nitride SiN_x and the oxide film SIO including silicon oxide SiO_x are sequentially deposited is disposed above the gate electrode 132 of the LTPS thin film transistor 130 and the gate electrode 142 of the oxide semiconductor thin film transistor 140.

[0083] Therefore, during the subsequent heat treatment process, movement of the hydrogen from the interlayer insulating layer 114 to the active layer 141 of the oxide semiconductor thin film transistor 140 may be suppressed.

[0084] Further, the oxide film SIO of the interlayer insulating layer 114 which is in directly contact with the active layer 141 of the oxide semiconductor thin film transistor 140 is formed of silicon oxide SiO_x having a low hydrogen content. Therefore, the influence due to hydrogen may be reduced as compared with a case in which the insulating layer which is formed of silicon nitride SiN_x is in directly contact with the active layer 141 of the oxide semiconductor thin film transistor 140.

[0085] Specifically, when an activating process and hydrogenating process on the active layer 131 of the LTPS thin film transistor 130 are not performed immediately after forming the interlayer insulating layer 114, but performed after forming the active layer 141 of the oxide semiconductor thin film transistor 140, more hydrogen may move from the interlayer insulating layer 114 to the active layer 141 of the oxide semiconductor thin film transistor 140 due to the high temperature which is applied at the time of the activating process and the hydrogenating process.

[0086] Therefore, in the organic light emitting display device 100 according to the exemplary embodiment of the present disclosure, the interlayer insulating layer 114 having a dual layered structure in which the nitride film SIN including silicon nitride SiN_x and the oxide film SIO

including silicon oxide SiO_x are sequentially deposited is used to reduce the diffusion of the hydrogen to the active layer 141 of the oxide semiconductor thin film transistor 140.

[0087] Accordingly, the reduction of the active layer 141 of the oxide semiconductor thin film transistor 140 is minimized and the change of the threshold voltage V_{th} of the oxide semiconductor thin film transistor 140 may be minimized.

[0088] Further, a contact hole may be formed in the gate insulating layer 113 and the interlayer insulating layer 114 to expose the source area SA and the drain area DA of the active layer 131 of the LIPS thin film transistor 130.

[0089] Next, the passivation layer 115 is entirely formed over the display area and the non-display area of the lower substrate 110.

[0090] Further, the passivation layer 115 is located on a top surface of the interlayer insulating layer 114 and is formed to cover the LIPS thin film transistor 130 and the oxide semiconductor thin film transistor 140 to be served as a protection layer. The passivation layer 115 may cover the signal line 170 with a patterned shape to minimize the generation of a crack in the non-display area of the lower substrate 110 at the time of bending.

[0091] The dummy metal pattern 150 is located on the top surface of the passivation layer 115. The dummy metal pattern 150 is configured by a storage capacitor electrode 151 which generates a storage capacitor C_{st} together with the source electrode 133 of the LTPS thin film transistor 130 and the dummy electrode 152 which serves as a second gate electrode of the oxide semiconductor thin film transistor 140. The dummy metal pattern 150 may be formed of the same material as the source electrode 133 of the LTPS thin film transistor 130.

[0092] The storage capacitor electrode 151 overlaps the source electrode 133 of the LTPS thin film transistor 130 and located with a large area. Further, the dummy metal pattern 150 generates a storage capacitor C_{st} together with the source electrode 133. The storage capacitor C_{st} may increase a capacity of the storage capacitor C_{st} using the storage capacitor electrode 151 with a large area so that the storage capacitor may be utilized for an organic light emitting display device which requires a high resolution.

[0093] The dummy electrode 152 is located above the oxide semiconductor thin film transistor 140. Further, the dummy electrode 152 is connected to the gate electrode 142 of the oxide semiconductor thin film transistor 140 through a contact metal pattern to be served as a second gate electrode of the oxide semiconductor thin film transistor 140. Therefore, the dummy electrode 152 may serve to shield the external light which is incident on the channel of the oxide semiconductor thin film transistor 140, which is advantageous for a bias temperature stress which is applied to the oxide semiconductor thin film transistor 140 element due to the manufacturing process.

[0094] Next, the planarization layer 116 is disposed on the passivation layer 115 on which the dummy metal pattern 150 is formed.

[0095] In the case of the organic light emitting display device 100 according to the exemplary embodiment of the present disclosure, after completing the LIPS thin film transistor 130 and the oxide semiconductor thin film transistor 140, the organic light emitting diode 160 may be formed. The organic light emitting diode 160 includes the

organic light emitting layer **162**. The organic light emitting layer **162** is desirably formed on a flat surface by the planarization layer **116**. The planarization layer **116** is disposed to planarize an upper surface of the lower substrate **110**. The planarization layer **116** may include an organic insulating material and may be thickly applied with a thickness of 5000 Å or larger.

[0096] Next, the organic light emitting diode **160** is located on the top surface of the planarization layer **116**. The organic light emitting diode **160** is configured by an anode electrode **161** which is a pixel electrode, the organic light emitting layer **162**, and a cathode electrode **163**.

[0097] The anode electrode **161** is electrically connected to the LTPS thin film transistor **130** which serves as a driving thin film transistor DT using a contact metal pattern among the dummy metal patterns **150**.

[0098] A bank **117** is formed on the planarization layer **116** on which the anode electrode **161** is formed. The bank **117** has a structure which exposes an emission area on the anode electrode **161** and covers the remaining part. Therefore, when the organic light emitting layer **162** is formed on the planarization layer **116** on which the bank **117** is formed, the organic light emitting layer **162** may be laminated so as to be in directly surface-contact with the anode electrode **161** which is exposed in the emission area. Thereafter, the organic light emitting diode **160** in which the anode electrode **161**, the organic light emitting layer **162**, and the cathode electrode **163** are laminated in the emission area may be completed by laminating the cathode electrode **163** on the organic light emitting layer **162**.

[0099] Next, the encapsulation unit **118** is formed on the organic light emitting diode **160**. Further, the encapsulation unit **118** is also located on the non-display area of the lower substrate **110**. The encapsulation unit **118** may serve to block undesirable foreign materials and moisture.

[0100] Finally, the signal line **170** is formed in the non-display area of the lower substrate **110**. The signal line **170** may be formed of the same material as the source and drain electrodes **143** and **144** of the oxide semiconductor thin film transistor **140**. Further, the signal line **170** is electrically connected to the gate driver **4** which transmits the driving signal to the pixel **1**.

[0101] FIG. 3 is a schematic flowchart illustrating a manufacturing process of a pixel illustrated in FIG. 1 according to an exemplary embodiment of the present disclosure. FIGS. 4A to 4C are cross-sectional views of a process for explaining a manufacturing method of a pixel illustrated in FIG. 1 according to an exemplary embodiment of the present disclosure. For instance, FIG. 3 and FIGS. 4A to 4C are a flowchart and a cross-section view of a process for explaining a manufacturing method of the pixel **1** of the organic light emitting display device **100** illustrated in FIG. 2 and a redundant description will be omitted or may be brief.

[0102] Referring to FIG. 3, first, a buffer layer **111** is formed on a lower substrate **110** (S1000).

[0103] Referring to FIG. 4A, the buffer layer **111** is deposited on a surface of the lower substrate **110**. Specifically, any one of silicon nitride SiN_x and silicon oxide SiO_x is deposited to form a single layered buffer layer **111** or silicon nitride SiN_x and silicon oxide SiO_x are alternately laminated to form a multiple layered buffer layer **111**.

[0104] Next, a BSM **120** is formed on the surface of the buffer layer **111** (S1010).

[0105] Referring to FIG. 4A, the BSM **120** is deposited on the buffer layer **111**. For example, the same material as the gate electrode **132** of the LIPS thin film transistor **130** is used to form a single layer BSM **120**.

[0106] Next, an active buffer layer **112** is formed on the buffer layer **111** (S1020).

[0107] Referring to FIG. 4B, the active buffer layer **112** is deposited on the surface of the buffer layer **111** so as to cover the BSM **120**. Specifically, any one of silicon nitride SiN_x and silicon oxide SiO_x is deposited to form a single layered active buffer layer **112** or silicon nitride SiN_x and silicon oxide SiO_x are alternately laminated to form a multiple layered active buffer layer **111**.

[0108] Next, the active layer **131** of the LIPS thin film transistor **130** is formed on the active buffer layer **112** (S1030).

[0109] Referring to FIG. 4B, an amorphous silicon (a-Si) is deposited on the surface of the active buffer layer **112** to form an a-Si layer (S1031), and perform dehydrating process on an a-Si layer (S1032). When there is a large amount of hydrogen in the a-Si layer, such hydrogen may create adverse effects during the subsequent crystalizing process (S1033), and thus cause failures. Therefore, the dehydrogenating step (S1032) is a process which removes the hydrogen from the a-Si layer and is carried out before performing the crystalizing process S1033 after forming the a-Si layer.

[0110] Next, referring to FIG. 3, after completing the dehydrogenating process S1032, a crystalizing process is performed on the a-Si layer (S1033).

[0111] The crystalizing process is a process which forms polysilicon by crystalizing the amorphous silicon (a-Si) of the a-Si layer, for example, may be performed by an excimer laser annealing (ELA) process.

[0112] Next, the p-Si layer on which the crystallization is completed is patterned to form the active layer **131** of the LIPS thin film transistor **130** (S1034).

[0113] Next, the gate insulating layer **113** of the LIPS thin film transistor **130** is formed (S1040) and the gate electrode **132** of the LIPS thin film transistor **130** and the gate electrode **142** of the oxide semiconductor thin film transistor **140** are formed (S1050).

[0114] Referring to FIG. 4B, the gate insulating layer **113** is formed on the active layer **131** of the LIPS thin film transistor **130**. Specifically, the gate insulating layer **113** may be formed of silicon nitride SiN_x or silicon oxide SiO_x. In consideration of stability and characteristic of the elements, the gate insulating layer **113** may have a thickness of approximately 1000 Å to 1500 Å. When the gate insulating layer **113** is formed of silicon nitride SiN_x, a large amount of hydrogen may be contained in the gate insulating layer **113** due to the manufacturing process. The hydrogen may diffuse to the outside of the gate insulating layer **113** in the subsequent process so that the gate insulating layer **113** may be formed of a silicon oxide (SiO_x) material.

[0115] Next, the gate electrode **132** of the LIPS thin film transistor **130** and the gate electrode **142** of the oxide semiconductor thin film transistor **140** are formed by depositing a material for a gate electrode on the gate insulating layer **113** and patterning the material for a gate electrode (S1050).

[0116] The material for a gate electrode may be various metal materials such as molybdenum (Mo).

[0117] Next, a doping process is performed on the active layer 131 of the LTPS thin film transistor with the gate electrode 132 of the LTPS thin film transistor 130 as a mask (S1060).

[0118] Referring to FIG. 4B, impurities are injected onto the active layer 131 of the LTPS thin film transistor 130 which is disposed at a lower portion using the gate electrode 132 of the LTPS thin film transistor 130 as a mask to define the source area SA and the drain area DA of the active layer 131 of the LTPS thin film transistor 130, that is, a doping area. The process of defining the doping area may vary by the P-MOS thin film transistor, the N-MOS thin film transistor, or the C-MOS thin film transistor.

[0119] For example, in the case of the N-MOS thin film transistor, the high density doping area is formed first and then the low density doping area may be formed. Specifically, the high density doping area is defined using a photoresist which is larger than the gate electrode 132 of the LTPS thin film transistor 130 and then the photoresist is removed. Further, the low density doping area LDD may be defined with the gate electrode 132 of the LTPS thin film transistor 130 as a mask.

[0120] In some exemplary embodiments, the doping area including the source area SA and the drain area DA may be defined before forming the gate insulating layer 113. Immediately after forming the active layer 131 of the LTPS thin film transistor 130, impurities may be doped using the photoresist.

[0121] Next, the interlayer insulating layer 114 is formed on the gate electrode 132 of the LTPS thin film transistor 130 and the gate electrode 142 of the oxide semiconductor thin film transistor 140 (S1070).

[0122] The interlayer insulating layer 114 is formed prior to a subsequent heat treatment process of an activating process and a hydrogenating process on the active layer 131 of the LTPS thin film transistor 130.

[0123] Referring to FIG. 4B, the interlayer insulating layer 114 may be formed to have a dual layered structure in which a nitride film SIN including silicon nitride SiN_x and an oxide film SIO including silicon oxide SiO_x are sequentially deposited.

[0124] The nitride film SIN of the interlayer insulating layer 114 diffuses hydrogen contained therein through the subsequent heat treatment process to be deposited to perform the hydrogenating process on the active layer 131 of the thin film transistor 130 containing the polycrystalline silicon.

[0125] In contrast, the oxidation film SIO of the interlayer insulating layer 114 is deposited in order to suppress hydrogen discharged from the nitride film SIN by the subsequent heat treatment process from being excessively diffused to the semiconductor material of the oxide semiconductor thin film transistor 140.

[0126] Next, the activating process is performed on the active layer 131 of the LTPS thin film transistor 130 (S1080) and the hydrogenating process is performed on the active layer 131 of the LTPS thin film transistor 130 (S1090).

[0127] First, the activating process on the active layer 131 of the LTPS thin film transistor 130 will be described. As a result of the doping process on the active layer 131 of the LTPS thin film transistor 130, the injected impurities (dopants) are present at random. Therefore, the activating process on the active layer 131 of the LTPS thin film transistor 130 is a process for placing the impurities in the silicon (Si)

lattice. Further, since the doping process on the active layer 131 of the LTPS thin film transistor 130 is a process of artificially injecting the impurities in the active layer, as a result of the doping process on the active layer 131 of the LTPS thin film transistor 130, the silicon Si may be damaged. Therefore, the activating process on the active layer 131 of the LTPS thin film transistor 130 is performed to cure the damage of the silicon Si.

[0128] Next, the hydrogenating process on the active layer 131 of the LTPS thin film transistor 130 will be described. The presence of vacancy in the polysilicon may degrade the characteristic of the polysilicon. Therefore, the hydrogenating process on the active layer 131 of the LTPS thin film transistor 130 is a process for filling vacancies of the polysilicon with hydrogen. The hydrogenating process on the active layer 131 of the LTPS thin film transistor 130 is performed by diffusing hydrogen included in the interlayer insulating layer 150 of the LTPS thin film transistor 130 by the heat treatment process. For example, the hydrogenating process may be performed through the heat treatment process at approximately 350° C. to 380° C. The active layer 131 of the LTPS thin film transistor 130 may be stabilized by the above-described hydrogenating process on the active layer 131 of the LTPS thin film transistor 130.

[0129] Next, the active layer 141 of the oxide semiconductor thin film transistor 140 is formed on the interlayer insulating layer 114 (S1100).

[0130] Referring to FIG. 3, a metal oxide, for example, IGZO is deposited on the interlayer insulating layer 114 to form an IGZO layer. In FIG. 3, it is described that the IGZO layer 1292 is formed under an assumption that the active layer 141 of the oxide semiconductor thin film transistor 140 is formed of IGZO among various metal oxides. However, the present disclosure is not limited thereto, but metal oxide other than IGZO may also be used.

[0131] The IGZO is deposited at a high temperature. Therefore, the IGZO may be crystallized during the IGZO deposition process. When the IGZO is deposited at a room temperature, the IGZO may be amorphous. However, when the IGZO is deposited at a high temperature, a layered structure of indium (In), gallium (Ga), and zinc (Zn) is formed to form a network. Further, as the crystallization is performed at the high temperature, oxygen vacancies are reduced in the IGZO layer. When there are many oxygen vacancies in the IGZO layer, a tunneling phenomenon is generated and thus the IGZO layer becomes conductive. Therefore, the BTS characteristic of the oxide semiconductor thin film transistor 140 are improved and the reliability is increased as the crystallization is performed a high temperature at the time of the IGZO deposition.

[0132] Next, the IGZO layer is thermally processed to stabilize the IGZO layer (S1102) and as illustrated in FIG. 4B, the IGZO layer is patterned (S1103) to form the active layer 141 of the oxide thin film transistor 140.

[0133] Next, the source electrode 133 and the drain electrode 134 of the LTPS thin film transistor 130 and the source electrode 143 and the drain electrode 144 of the oxide semiconductor thin film transistor 140 are formed (S1110).

[0134] As illustrated in FIG. 4B, the source electrode 133 of the LTPS thin film transistor 130 is electrically connected to the BSM 120 through the contact holes of the interlayer insulating layer 114, the gate insulating layer 113, and the active buffer layer 112. Further, when the source electrode 133 and the drain electrode 134 of the LTPS thin film

transistor **130** and the source electrode **143** and the drain electrode **144** of the oxide semiconductor thin film transistor **140** are formed, a signal line **170** is formed of the same material as the source electrode and the drain electrode in the non-display area of the lower substrate **110**.

[0135] Referring to FIG. 4B, the source electrode **133** and the drain electrode **134** of the LIPS thin film transistor **130** and the source electrode **143** and the drain electrode **144** of the oxide semiconductor thin film transistor **140** are formed by depositing and patterning a material for the source electrode and the drain electrode on the gate insulating layer **114** and the active layer **141** of the oxide semiconductor thin film transistor **140**. In this case, the source electrode **133** and the drain electrode **134** of the LIPS thin film transistor **130** and the source electrode **143** and the drain electrode **144** of the oxide semiconductor thin film transistor **140** are formed of a triple layered structure of titanium (Ti)/aluminum (Al)/titanium (Ti) so that the patterning process may be performed by dry etching. Further, by the patterning process of the source electrode **143** and the drain electrode **144**, a groove is formed in a part of the buffer layer **111** formed in the non-display area of the lower substrate **110** and the remaining insulating layers are removed.

[0136] In some exemplary embodiment, in order to suppress the damage of the active layer **141** of the oxide semiconductor thin film transistor **140**, two steps of dry etching are applied to perform a primary dry etching at a high etching rate and perform a secondary dry etching at a low etching rate. Therefore, the damage of the active layer **141** of the oxide semiconductor thin film transistor **140** may be reduced.

[0137] Next, a passivation layer **115** is formed to cover the LIPS thin film transistor **130** and the oxide semiconductor thin film transistor **140** (S1120).

[0138] The passivation layer **115** may be formed of silicon nitride SiN_x or silicon oxide SiO_x. Next, the passivation layer **115** is entirely formed over the display area and the non-display area of the lower substrate **110**. Specifically, the passivation layer **115** formed in the non-display area encloses the signal line **170**. It is considered that the passivation layer **115** protects the signal line **170**.

[0139] Next, the dummy metal pattern **150** is formed on a surface of the passivation layer **115** (S1130).

[0140] Referring to FIG. 4C, the dummy metal pattern **150** is configured by a storage capacitor electrode **151** which generates a storage capacitor C_{st} together with the source electrode **133** of the LIPS thin film transistor **130** and the dummy electrode **152** which serves as a second gate electrode of the oxide semiconductor thin film transistor **140**. The dummy metal pattern **150** may be formed of the same material as the source electrode **133** of the LIPS thin film transistor **130**.

[0141] Next, when the dummy metal pattern **150** is formed by dry etching, the passivation layer **115** which is formed in the non-display area of the lower substrate **110** is also patterned (S1140).

[0142] As a result, when a part of the non-display area is bent, the crack generation may be minimized.

[0143] Next, a planarization layer **116** is formed on the passivation layer **115** and the dummy metal pattern **150** (S1150) and the anode electrode **161** of the organic light emitting diode **160** is formed on the planarization layer **116** (S1160). The bank **117** is formed on the planarization layer **116** and the anode electrode **161** (S1170), the organic light

emitting layer **162** is formed on the top surface of the anode electrode (S1180), and the cathode electrode **163** is formed on the top surface of the organic light emitting layer (S1190).

[0144] Referring to FIG. 4C, the planarization layer **116** which is formed in the non-display area is removed at the time of the process of patterning the organic light emitting diode **160**.

[0145] Finally, an encapsulation unit **190** is formed on the organic light emitting diode (S1200).

[0146] Some of the features of the embodiment(s) of the present disclosure can be described as follows.

[0147] According to an aspect of the present disclosure, the dummy electrode of the organic light emitting display device according to an exemplary embodiment of the present disclosure is connected to the second gate electrode using a contact metal pattern which is formed of the same material as the second source electrode and is located on the same plane as the second source electrode.

[0148] The organic light emitting display device may further include a lower protective metal pattern on the first buffer layer. The lower protective metal pattern is disposed to overlap the driving transistor.

[0149] The lower protective metal pattern of the organic light emitting display device may be electrically connected to the first source electrode to minimize a current drop of the driving transistor.

[0150] The organic light emitting display device may further include a second buffer layer on the lower protective metal pattern in the display area of the organic light emitting display device.

[0151] The organic light emitting display device may further include a signal line unit formed of the same material as the first source electrode and on the same plane as the first source electrode in the non-display area.

[0152] The organic light emitting display device may further include a passivation layer to cover the driving transistor and the switching transistor.

[0153] A capacitor electrode and a dummy electrode are located on the passivation layer of the organic light emitting display device.

[0154] The passivation layer of the organic light emitting display device is formed over the display area and the non-display area.

[0155] The passivation layer of the organic light emitting display device has a pattern shape which minimizes cracks generated in the non-display area at the time of bending.

[0156] The first buffer layer of the organic light emitting display device has a groove in a partial area of the non-display area.

[0157] The flexible substrate of the organic light emitting display device can be made of polyimide.

[0158] The first gate electrode and the second gate electrode of the organic light emitting display device are simultaneously formed on the same plane.

[0159] The second gate electrode and the dummy electrode of the organic light emitting display device shield external light which is incident onto the upper portion and the lower portion of the channel of the switching transistor.

[0160] The dummy electrode of the organic light emitting display device may minimize a bias temperature stress (BTS) of the switching transistor.

[0161] The organic light emitting display device may further include a gate driving thin film transistor which is

located in the non-display area of the organic light emitting display device and is electrically connected to a part of the signal line unit.

[0162] The gate driving thin film transistor of the organic light emitting display device has the polycrystalline silicon (LTPS) layer as an active layer.

[0163] The organic light emitting display device may further include a gate insulating layer which insulates a polycrystalline silicon (LTPS) layer of the driving transistor and the first gate electrode from each other.

[0164] The organic light emitting display device may further include an interlayer insulating layer on a top surface of the gate insulating layer. The interlayer insulating layer is configured to cover the first gate electrode and the second gate electrode.

[0165] The interlayer insulating layer of the organic light emitting display device may have a dual layered structure in which a nitride film SIN including silicon nitride SiN_x and an oxide film SIO including silicon oxide SiO_x are sequentially deposited.

[0166] The oxide film SIO of the organic light emitting display device may minimize hydrogen which is discharged from the nitride film SIN due to a subsequent heat treatment process from being diffused to the oxide semiconductor layer of the switching transistor.

[0167] The exemplary embodiments of the present disclosure have been described with reference to the accompanying drawings, but those skilled in the art will understand that the present disclosure may be implemented in other specific forms without changing the technical scope thereof. Thus, it is to be appreciated that embodiments described above are intended to be illustrative in every sense, and not restrictive. Further, the scope of the present disclosure may be indicated by the following claims rather than the above detailed description. It should be interpreted that all changes or modifications deduced from the meaning and the scope of the claims and the equivalent concepts thereof are included in the scope of the present disclosure.

What is claimed is:

1. An organic light emitting display device, comprising:
 - a flexible substrate including a display area and a non-display area;
 - a first buffer layer over an entire surface of the flexible substrate;
 - a driving transistor on the first buffer layer in the display area, the driving transistor including a polycrystalline silicon (LTPS) layer, a first gate electrode, a first source electrode, and a first drain electrode;
 - a capacitor electrode on the first source electrode of the driving transistor, the capacitor electrode forming a storage capacitor together with the first source electrode;
 - a switching transistor in the display area to be spaced apart from the driving transistor, the switching transistor including an oxide semiconductor layer, a second gate electrode, a second source electrode, and a second drain electrode; and
 - a dummy electrode on the switching transistor, the dummy electrode formed of the same material as the capacitor electrode, disposed on the same plane as the capacitor, and functioning as a third gate electrode of the switching transistor.
2. The organic light emitting display device according to claim 1, wherein the dummy electrode is connected to the

second gate electrode through a contact metal pattern, the contact metal pattern formed of the same material as the second source electrode and located on the same plane as the second source electrode.

3. The organic light emitting display device according to claim 1, further comprising:

- a lower protective metal pattern on the first buffer layer and disposed to overlap the driving transistor.

4. The organic light emitting display device according to claim 3, wherein the lower protective metal pattern is electrically connected to the first source electrode to minimize a current drop of the driving transistor.

5. The organic light emitting display device according to claim 3, further comprising:

- a second buffer layer on the lower protective metal pattern in the display area.

6. The organic light emitting display device according to claim 1, further comprising:

- a signal line unit formed of the same material as the first source electrode and on the same plane as the first source electrode in the non-display area.

7. The organic light emitting display device according to claim 1, further comprising:

- a passivation layer covering the driving transistor and the switching transistor.

8. The organic light emitting display device according to claim 7, wherein the capacitor electrode and the dummy electrode are located on the passivation layer.

9. The organic light emitting display device according to claim 7, wherein the passivation layer is formed over the display area and the non-display area.

10. The organic light emitting display device according to claim 9, wherein the passivation layer has a pattern shape which minimizes cracks generated in the non-display area when the non-display area is bent.

11. The organic light emitting display device according to claim 1, wherein the first buffer layer has a groove in a partial area of the non-display area.

12. The organic light emitting display device according to claim 1, wherein the flexible substrate is formed of polyimide.

13. The organic light emitting display device according to claim 1, wherein the first gate electrode and the second gate electrode are formed on the same plane as a result of the same manufacturing process.

14. The organic light emitting display device according to claim 1, wherein the second gate electrode and the dummy electrode shield external light which is incident onto an upper portion and a lower portion of a channel of the switching transistor.

15. The organic light emitting display device according to claim 1, wherein the dummy electrode minimizes a bias temperature stress (BTS) of the switching transistor.

16. The organic light emitting display device according to claim 6, further comprising:

- a gate driving thin film transistor in the non-display area, the gate driving thin film transistor electrically connected to a part of the signal line unit.

17. The organic light emitting display device according to claim 16, wherein the gate driving thin film transistor has the polycrystalline silicon (LTPS) layer as an active layer.

18. The organic light emitting display device according to claim 1, further comprising:

a gate insulating layer insulating the polycrystalline silicon (LTPS) layer and the first gate electrode from each other.

19. The organic light emitting display device according to claim **18**, further comprising:

an interlayer insulating layer on a top surface of the gate insulating layer, the interlayer insulating layer covering the first gate electrode and the second gate electrode.

20. The organic light emitting display device according to claim **19**, wherein the interlayer insulating layer has a dual layered structure in which a nitride film (SIN) including silicon nitride (SiN_x) and an oxide film (SIO) including silicon oxide (SiO_x) are sequentially deposited.

21. The organic light emitting display device according to claim **20**, wherein the oxide film (SIO) minimizes hydrogen being diffused into the oxide semiconductor layer of the switching transistor which is discharged from the nitride film (SIN) due to a subsequent heat treatment process.

22. An organic light emitting display device, comprising:
a flexible substrate including a display area and a non-display area;

a driving transistor in the display area, the driving transistor having a polycrystalline silicon (LTPS) layer as an active layer; and

a switching transistor in the display area, the switching transistor disposed to be spaced apart from the driving transistor,

wherein the switching transistor includes:

a first gate electrode;

an oxide semiconductor layer overlapping the first gate electrode;

a first source electrode in contact with one side of the oxide semiconductor layer;

a first drain electrode in contact with another side of the oxide semiconductor layer; and

a second gate electrode connected to the first gate electrode.

23. The organic light emitting display device according to claim **22**, wherein the driving transistor further includes a third gate electrode, a second source electrode, and a second drain electrode.

24. The organic light emitting display device according to claim **23**, further comprising:

a dummy metal pattern formed of the same material as the second gate electrode and on the same plane as the second gate electrode, the dummy metal pattern disposed to overlap the third gate electrode.

25. The organic light emitting display device according to claim **24**, wherein the dummy metal pattern forms a storage capacitor together with the second source electrode.

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